



230729 – CONFIGURABLE DIGITAL ELECTRONICS

Credits: 5 ECTS

LECTURER

Coordinating lecturers: Joan Pons, Juan Antonio Chávez

Others: Marco Azpurúa

PRIOR SKILLS

Fundamentals of digital electronics: number systems, binary codes, Boolean Algebra, analysis and design of combinational circuits, combinational modules, analysis and design of simple sequential circuits, sequential modules (registers, counters, etc.) Fundamentals of CMOS technology.

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Transversal:

TEAMWORK. Being able to work as a member of an interdisciplinary team, either as a member or carrying out management tasks, in order to contribute to developing projects with pragmatism and a sense of responsibility, assuming commitments taking into account the available resources.

EFFECTIVE USE OF INFORMATION RESOURCES: Managing the acquisition, structuring, analysis and display of data and information in the chosen area of specialisation and critically assessing the results obtained.

FOREIGN LANGUAGE: Achieving a level of spoken and written proficiency in a foreign language, preferably English, that meets the needs of the profession and the labour market.

TEACHING METHODOLOGY

- Lectures
- Laboratory classes
- Personal work (distance)
- Short answer tests (midterm exams)
- Extended answer test (Final Exam)

LEARNING OBJECTIVES OF THE SUBJECT

Learning objectives of the subject:

The aim of this course is the presentation and use of advanced digital design tools and methodologies, with especial emphasis on hardware description languages, programmable logic devices and advanced design techniques for medium-complexity digital subsystems.



Learning results of the subject:

- Analysis and design of synchronous digital circuits of medium complexity.
- Application of the fundamentals of hardware description languages.
- Use of programmable logic devices, FPGAs.
- Evaluation of performance of synchronous digital circuits.

STUDY LOAD

Hours large group: 13

Hours small group: 26

Hours self-study: 86

CONTENTS

To be detailed in lessons and some points within every lesson. Time dedicated for every lesson is also indicated.

The theory classes are grouped in three theory modules (TMs), as follows:

- TM1: Introduction to VHDL
 - Lesson 1: VHDL fundamentals, data types, data objects and operators.
 - Lesson 2: Basic design units: entities, architectures, packages and libraries.
 - Lesson 3: Dataflow modelling: concurrent assignments.
 - Lesson 4: Behavioural modelling: processes and sequential assignments.
 - Lesson 5: Structural modelling: components, generation and iteration statements.

Theory classes: 5h
Self-study : 20h
- TM2: Digital design topics
 - Lesson 1: Finite State Machines: review, specification with VHDL, synthesis.
 - Lesson 2: Logic hazards: static and dynamic glitches, effects and mitigation strategies.
 - Lesson 3: Power consumption: static and dynamic power, current spikes, power estimation in CPLDs and FPGAs, low power strategies.
 - Lesson 4: Metastability and timing: metastability in synchronous circuits, synchronization errors, evaluating synchronization strategies: mean time between failures.
 - Lesson 5: About synchronous design: evaluating time performance of sync. circuits, the sync./async. trade-off, connecting sync. & async. circuits, concurrent FSMs.

Theory classes: 5h
Self-study : 20h
- TM3: Algorithmic systems
 - Lesson 1: Fundamentals of Algorithmic State Machines, data & control subsystems, ASM chart and VHDL specification, timing involved.
 - Lesson 2: Design of specific data and control units.
 - Lesson 3: Microprogrammed control: simple and evolved memory-based control units.

Theory classes: 3h
Self-study : 12h

The laboratory classes are grouped in three lab modules (LMs), as follows:

- LM1: Introduction to the laboratory tools for designing with FPGAs. The initial work to be done consists of implementing an already-given basic design step by step, following a tutorial procedure. The second part consists of making improvements and extensions to the previous design, as chosen by the student.



Laboratory classes: 8h

Self-study : 8h

- LM2: VHDL hierarchical design. The initial work to be done consists of analysing the structure and operation of a complex digital system, specifically a keyboard reader and sequence analyser given in the form of several VHDL modules. Later, it is proposed to correct any errors found in the design of the system and to make improvements or extensions to it.

Laboratory classes: 8h

Self-study : 12h

- LM3: Project design. The work to be done consists of specifying, simulating and implementing a complex design, which includes working on concepts such as: the interaction of the FPGA with peripherals (such as LCD displays), the use of external memory blocks or basic data communication (such as serial transmission), the use of IPs, etc. The LM2 system or designs proposed by the students themselves can be taken as a starting point.

Laboratory classes: 10h

Self-study : 16h

GRADING SYSTEM

The final grade for the course is 60% for the laboratory part plus 40% for theory part.

The laboratory mark is 75% of the LMs plus 25% of a specific laboratory exam.

The theory mark is the maximum between:

- The note of the final exam of theory

- 50% from the theory exam plus another 50% from two short exams and the exercises to be done at home during the semester.

BIBLIOGRAPHY

Basic:

- Balch, M. Complete digital design: a comprehensive guide to digital electronics and computer system architecture. New York: McGraw-Hill, 2003. ISBN 978-0071737708.
- Zwolinski, M. Digital system design with VHDL. 2nd ed. Harlow, England: Prentice-Hall, 2004. ISBN 013039985X.

Complementary:

- Rushton, A. VHDL for logic synthesis [on line]. 3rd ed. Wiley, 2011 [Consultation: 21/06/2017]. Available on: <http://onlinelibrary.wiley.com/book/10.1002/9781119995852>. ISBN 9781119995852.
- Lee, S. Advanced digital logic design: using VHDL, state machines, and synthesis for FPGAs. Southbank: Thomson, 2006. ISBN 978-0534466022.